A Fully Integrated 40-Gbit/s Clock and Data Recovery Circuit Using InP/InGaAs HBTs

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Abstract — **An integrated clock and data recovery (CDR) circuit is a key element for optical communication systems at 40 Gbit/s. We present a fully integrated 40-Gbit CDR circuit fabricated using InP/InGaAs HBTs. The circuit contains a linear-type phase detector and a full-data-rate voltage-controlled oscillator. Error-free operation and wide eye opening were obtained for 40-Gbit/s pseudorandom bit sequence (PRBS) with a length of 2^{23}-1. The fabricated IC dissipates 1.71 W at a supply voltage of –4.5V.**

I. Introduction

A clock and data recovery (CDR) circuit is required in an optical receiver in order to extract the clock signal from the incoming random data stream. To meet the increasing demands for more transmission capacity, time-division multiplexing (TDM) systems at a data rate of 40 Gbit/s are now under development. 40-Gbit/s class monolithic integrated CDRs using SiGe bipolar [1] and GaAs HEMT [2] technologies have been reported. These CDRs, however, use half-data-rate clocks to regenerate the input data. While the half-rate architecture has an advantage of half-speed circuit operation, it requires about twice the circuit scale and quadrature clock phases. Recently, full-data-rate CDRs have been demonstrated by using InP-based devices. Murata et al. [3] reported a fully integrated 43-Gbit/s CDR IC using InP-HEMTs. On the other hand, only open-loop operation has been verified in the full-data-rate CDR using InP HBTs [4].

HBTs have some advantages over HEMTs in terms of driving capability, breakdown voltage, and device size. Concerning CDR applications, the lower phase noise [5] and higher driving capability [6] of HBTs result in lower jitter generation in voltage-controlled oscillators (VCOs) and higher input sensitivity in decision circuits, respectively. Among HBTs, InP-based HBTs are superior to GaAs-based HBTs in terms of speed and power dissipation because of high electron velocities and low base-emitter turn-on voltages [7].

This paper describes a fully integrated 40-Gbit/s CDR circuit fabricated using InP/InGaAs HBTs [8]. Error-free operation was obtained for 40-Gbit/s pseudorandom bit sequence (PRBS) with a length of 2^{23}-1. To our knowledge, this is the first demonstration of 40-Gbit/s full data rate CDR using HBTs.

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II. Circuit Design

Figure 1 shows a block diagram of the CDR circuit. It consists of a half-bit delay, a linear-type phase detector (PD), a lag-lead loop filter, a feed-forward-type VCO, a master-slave D-type flip-flop (D-FF), and output drivers. The phase-locked-loop (PLL) based architecture of the CDR is consistent with that in [9]. The linear-type PD offers a wide pull-in range without a frequency acquisition circuit, whereas the binary-type PD tends to limit loop gain and pull-in range to prevent jitter caused by the so-called bang-bang operation. In addition, the linear CDR architecture contains only one clock distribution (to the D-FF and the output driver) because the linear-type PD detects clock phases indirectly from incoming data and retimed data. This eases the layout-design difficulty that we face when the binary CDR is used for such high-speed operation.

The half-bit delay, which roughly compensates data edge density variations, is composed of two-stage differential amplifiers. A static master-slave D-FF is used as the decision circuit to obtain good retiming feature. Figure 2 shows

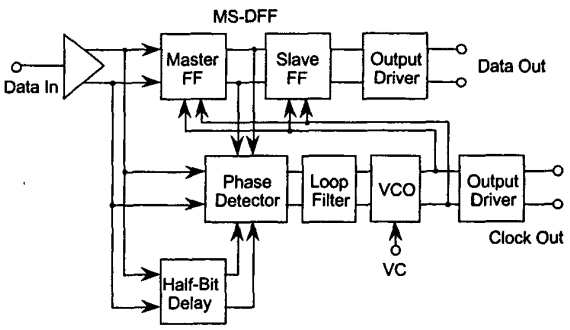
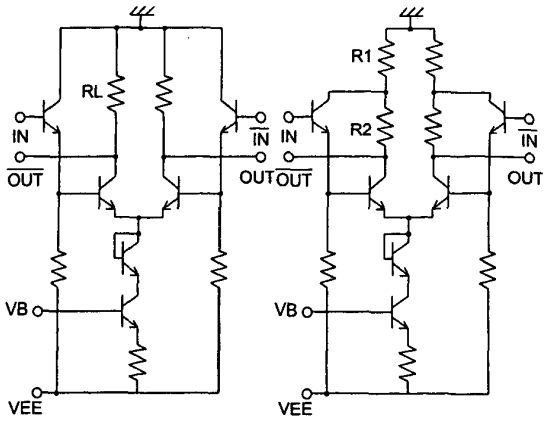
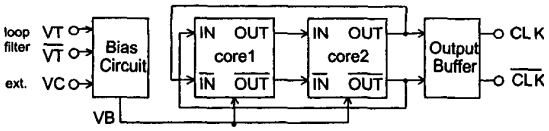


Fig. 1. Block diagram of the CDR circuit.



(a) normal-type VCO core (b) feed-forward-type VCO core



(c) VCO configuration

Fig. 2. Ring-oscillator-type VCO.

the VCO configuration. A two-stage ring oscillator was used as the VCO. To boost oscillation frequency without reducing internal voltage amplitude, we adopted novel feed-forward differential amplifiers as VCO cores. A similar technique has been demonstrated in a T-type flip-flop [10] to improve the operation frequncy. Figure 3 shows the simulated oscillation frequency versus the internal voltage amplitude under the condition that VB is constantly biased near the maximum oscillation frequency. The feed-forward ratio (FFR) is defined as (R1 / RL) x 100, where RL = R1 + R2. The oscillation frequency is in a trade-off relation with the internal voltage amplitude in the case of FRR = 0% (normal-type VCO core). The relationship is relaxed with increasing FRR. In this design, we selected a FFR of 50% with a RL of 110 Ω to reach 40 GHz.

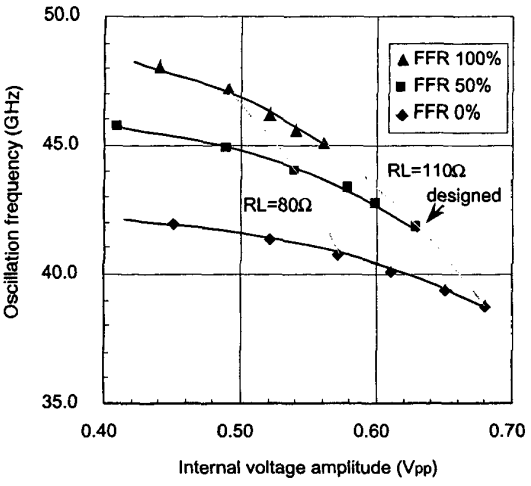


Fig. 3. Simulated VCO oscillation frequency.

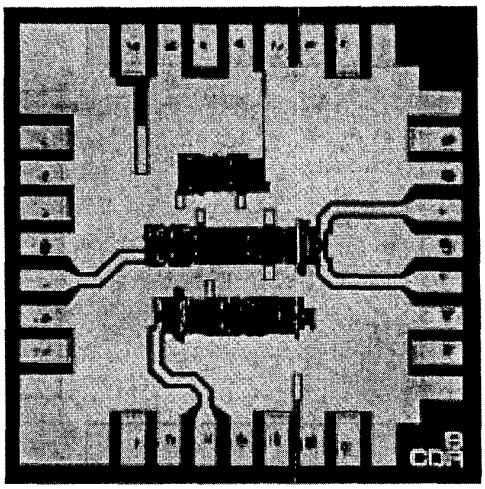


Fig. 4. Photograph of the CDR IC.

III. Experimental Results

The CDR IC was fabricated using non-self-aligned InP/InGaAs HBTs [8]. The epitaxial layers were grown on 3-inch wafer by metalorganic vapor phase epitaxy (MOVPE). The HBT has a 70-nm-thick undoped InP emitter, a 50-nm-thick carbon-doped InGaAs base, and a 300-nm-thick InGaAs collector. The lateral emitter dimension of the standard HBT is 1 μm x 4 μm. The undoped emitter offers the same cut-off frequency f_T as the conventional emitter structure at only half the collector current. The fabricated HBTs have a f_T of 140 GHz, and a f_{max} of 200 GHz at the current density of 5 x 10^4 A/cm^2 with V_{CE} = 1.2 V. Figure 4 shows the photograph of the CDR IC. The chip size is 2 mm x 2 mm.

Measurements were performed on wafer using quadruple RF probes. The input 40-Gbit/s nonreturn-to-zero signal was generated by the combination of a 12.5-Gbit/s 4-channel pulse pattern generator (PPG), a 25-Gbit/s multiplexer unit, and a multiplexer module with a 70-Gbit/s multiplexer and a 50-Gbit/s decision circuit using InP HEMTs [11]. The recovered data signal from the CDR IC

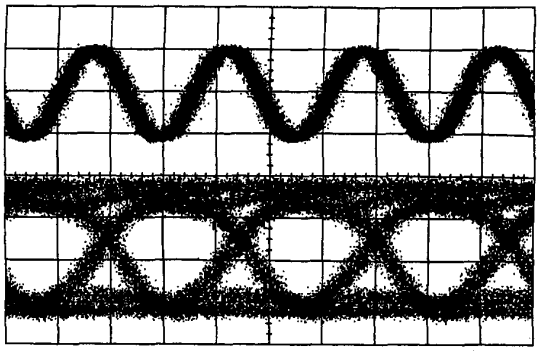


Fig. 5. Measured waveforms of recovered clock (upper) and recovered data (lower). H: 10 ps/div., V: 200 mV/div.

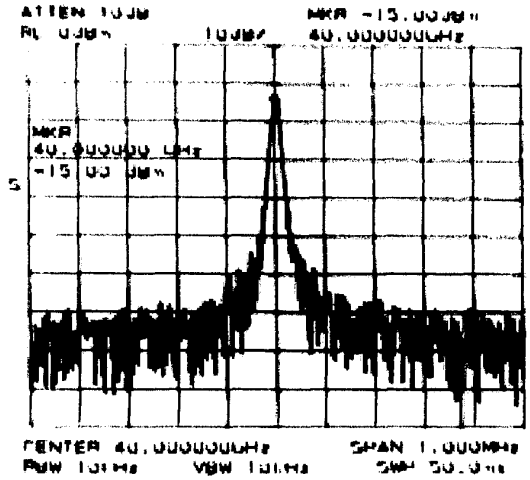


Fig. 6. Measured spectrum of recovered clock.

was demultiplexed twice using an InP HEMT decision IC module [11], and then sent to an error detector.

Figure 5 shows the waveforms of recovered clock (upper trace) and recovered data (lower trace) observed by a digitized sampling oscilloscope (HP 54750A). The input data was a 40-Gbit/s 2^{23}-1 PRBS. The eye opening was very wide, and error-free operation was confirmed. The rms jitter of recovered clock and recovered data measured by the oscilloscope were 0.9 and 1.3 ps, respectively. The VCO oscillation frequency can be adjusted from 31.5 to 40.3 GHz by controlling VC. The VCO exhibits a wide tuning range of 25% around its midband frequency. The CDR operation was confirmed almost throughout the complete VCO tuning range using a 0011 data pattern from a frequency synthesizer. The pull-in range of the CDR was

TABLE I
COMPARISON OF THE CDR ICs

Ref.	Device	Bit rate	Power dis.	Comment
[1]	SiGe HBT	40 Gbit/s	5.4 W	with 1:4 DEMUX, half-rate clock
[2]	GaAs HEMT	40 Gbit/s	3.2 W	with 1:4 DEMUX, half-rate clock
[3]	InP HEMT	43 Gbit/s	2.79 W	
[4]	InP HBT	40 Gbit/s	5.6 W	only open-loop operation
This work	InP HBT	40 Gbit/s	1.71 W	

TABLE II
CDR IC CHARACTERISTICS

Technology	InP/InGaAs HBT with undoped emitter (f_T = 140 GHz, f_{max} = 200 GHz)
Chip size	2 mm x 2 mm
Supply voltage	-4.5 V
Power dissipation	1.71 W
Recovered clock jitter	946 fs_{RMS}, 6.67 ps_{p-p} for 2^{23}-1 PRBS
	848 fs_{RMS}, 6.00 ps_{p-p} for 2^7-1 PRBS
Recovered data jitter	1277 fs_{RMS}, 9.56 ps_{p-p} for 2^{23}-1 PRBS
	1292 fs_{RMS}, 9.11 ps_{p-p} for 2^7-1 PRBS
Output amplitude	440 mV_{p-p} for recovered clock
	640 mV_{p-p} for recovered data
Pull-in range	105 MHz
VCO tuning range	31.5 GHz-40.3 GHz (25%)
Input sensitivity*	30 mV (BER < 10^{-12}, 2^{23}-1 PRBS)

* Measured at 36 Gbit/s

estimated at 105 MHz by using a measured VC-pull-in range of 9.8 mV and a measured VCO sensitivity against VC of 10.7 GHz/V for the condition of 40 Gbit/s, 2^7-1 PRBS, and BER < 10^{-10}. Figure 6 shows the spectrum of the recovered clock. The power dissipation of the IC was 1.71 W at a supply voltage of –4.5 V. Table I compares the power dissipation of the CDR ICs reported in [1]-[4]. The InP-HBTs we used for the CDR IC have a potential for fabricating a 1.8-W 1:4 DEMUX. We estimate that the power dissipation of the CDR with 1:4 DEMUX IC should be lower than 3 W by taking account of the removal of CDR output drivers and a DEMUX input buffer. Table II summarizes the measured characteristics of the CDR IC.

IV. CONCLUSION

A fully integrated 40-Gbit/s CDR IC was realized using InP/InGaAs HBTs. The CDR IC regenerates incoming data by a static decision circuit at a full-data-rate recovered clock. Error-free operation and wide eye open-

ing were obtained for a 40-Gbit/s 2^{23}-1 PRBS data signal. Low-power dissipation of 1.71 W was achieved by using undoped-emitter HBTs and a linear-PLL architecture.

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